Vectorizing Database Column Scans with Complex **Predicates**

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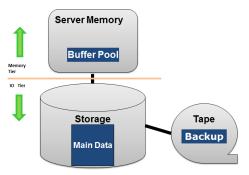








Traditional Architecture



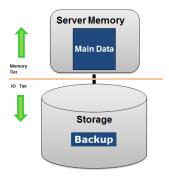
 Memory has become large enough to contain all data.







In-memory Architecture



- Keeping data in memory allows faster access to data, overcomes disk latency.
- Backup is kept on storage.









Disruptive change in RDBMS industry

- Rise of In-Memory Databases (IMDBs).
- Anticipated by research 10+ years ago.
- All major DB vendors are working on it.
- SAP leading with HANA as platform for all new apps.

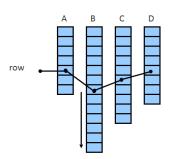








IMDBs often use Column-Orientation



Advantages of column-orientation:

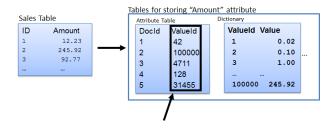
- Columns compressed independently
- Leverages better compression
- Cache-friendly:
 - cache-line granularity
 - prefetching
- SIMD-friendly











- "Dictionary" contains all distinct values (e.g. 100,000 entries)
- Valueld are integers from 0, 1, 2, 3, ..., 100000
- Max is N=100000 (number of distinct values), which needs 17 bits to represent ([log₂N] + 1)
- Idea: instead of 32-bits, use 17-bits fields to store each ValueID.
 We then call "17" the "Bit-case"
- Accessing "Value" needs decompression into 32-bits



Compression building blocks: Bit-Fields

Packed bit-fields

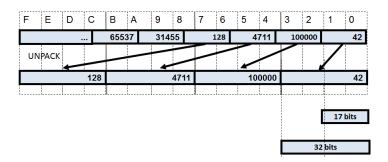
• Large number of integers, each with n number of bits

F	Е	D	С	В	Α	9	8	7	6	5	4	3	2	1	0
128			4711				100000						42		
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Compression building blocks: Bit-Fields

Packed bit-fields

- Large number of integers, each with n number of bits
- Example: 17-bit per entry:



32 different implementations for each n from 1 to 32.



For each query do a full-table scan, i.e.,

- Decompress required columns,
- Aggregate data according to predicate,
- Further processing.

Performance of unpacking is key for full-table scans!







Vectorized Scan Framework: Overview

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- Different classes of predicates:
 - Range predicates
 - Vectorizable predicates
 - In-list predicates
 - Arbitrary predicates









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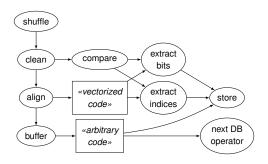
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- Different classes of predicates:
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 - Arbitrary predicates
- Different output formats:
 - Bit vectors
 - Index vectors
 - Unpacked data





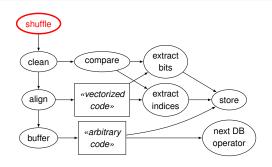


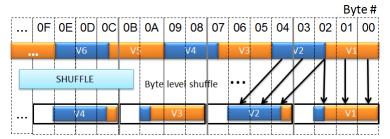


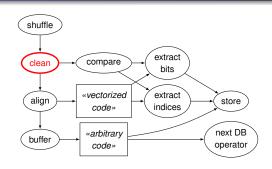


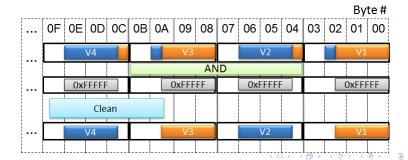
- Common scheme for all predicates and output formats
- Extensible with templates
- Vectorized processing of 8 values at a time (or more)
- Manual optimizations of all paths and all bit cases

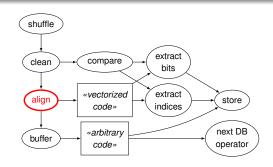


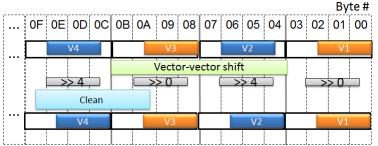


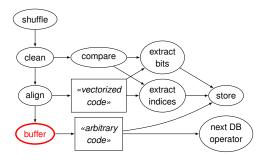




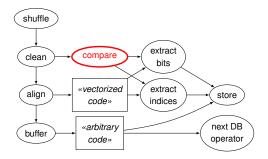




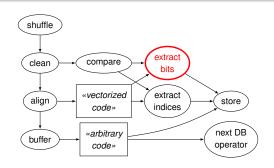


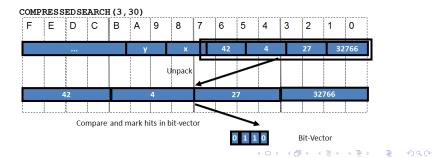


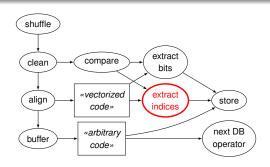
Write to Buffer

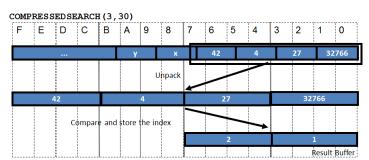


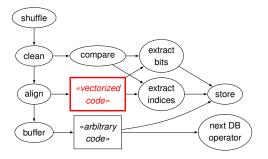
• Range predicates (can express all the equality predicates, i.e., =, \neq , >, >, <, <)





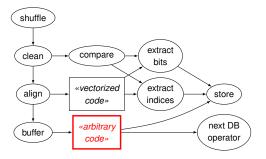




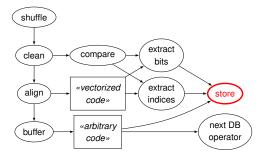


Many other predicates, including many arithmetic expressions on a single column, can easily be expressed using vector instructions.

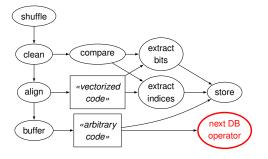
Example: In-list predicate.



Fall-back mechanism, where a block of codewords is unpacked as machine words into a buffer in cache, on which arbitrary predicates can be applied.



Store the different classes of results



Unpack a columm for the subsequent database operator.

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Example: Scan algorithm for In-list predicate



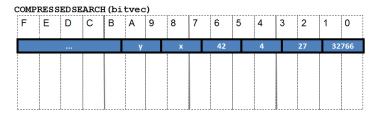






Search the values that are marked in a bitvector:

- 1 UNPACK
- 2 If corresponding bit is set
- 3 Mark bit in result bitvector

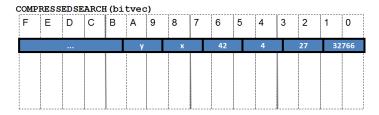






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Predicate Bit-Vector

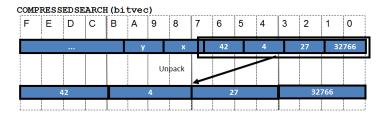






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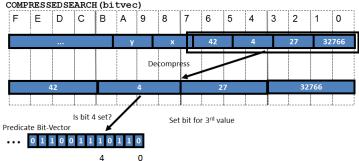
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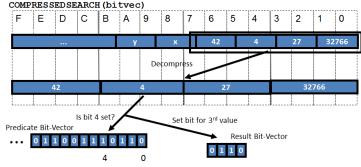


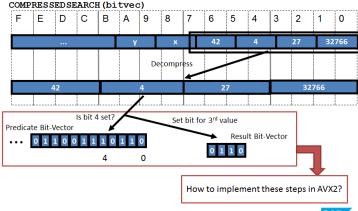




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Two AVX2 instructions are key to achieve the parallelization of the Scan with in-list predicate algorithm:

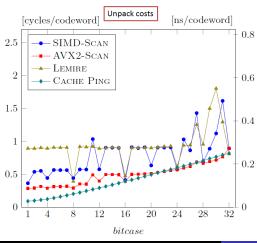
- Vector-vector shift instruction: The new vector-vector shift instructions allows shifting each word of the AVX register with an independent value. We use it to convert the values into words where only the bit at the index equal to the value is set to 1.
- Gather instruction: The new gather instructions loads elements from memory based on a base address and offsets for each data element. We use it to gather the different chunks of the predicate relevant to vectorized comparison.







Evaluation: Unpack Performance



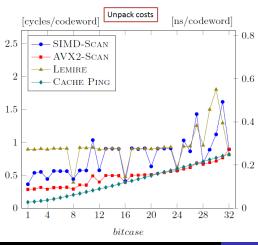
- Bit cases have different performances due to different optimizations.
- Example: bit case 16 is trivially easy.
- AVX2-Scan is 30% faster than SIMD-Scan
- Bit cases >16 are memory bound.







Evaluation: Unpack Performance



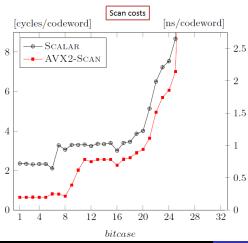
- Lemire's reimplemation of SIMD-Scan often matches our performance, but we found additional optimizations.
- Li's reimplemantation needs 5 cycles/codeword.







Evaluation: Scan Performance



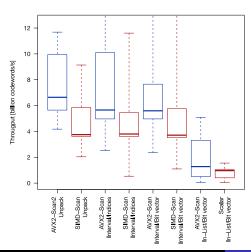
- Optimizations "Permute" and "AvoidGather" work very well for bitcases <= 8.
- In these cases 4 times faster than Scalar.
- Bit cases >21 and >26 get penalties from L2 and L3 cache misses for the bit-vector predicate.







Evaluation: Throughtput Overview



- AVX2-Scan consistently 30% faster than SIMD-Scan.
- Throughputs between 4 and 10 billion codewords per second with peaks of 17 billion.









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 - Compress instruction.
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 - 512 bit registers.
 - Mask registers.
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 - Compress instruction.
 - Unsigned comparison.
- It would be interesting to compare our approach with GPUs.







